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(54) **THIN-FILM TRANSISTOR ARRAY  
SUBSTRATE AND ORGANIC  
LIGHT-EMITTING DISPLAY INCLUDING  
THE SAME**

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(57) **ABSTRACT**

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A thin-film transistor (TFT) array substrate includes a substrate, a gate-underlying stepped layer disposed on the substrate, a gate electrode disposed on the gate-underlying stepped layer, a semiconductor layer formed over the gate electrode, and an etch-stopper disposed on the semiconductor layer. The gate-underlying stepped layer is formed under the gate electrode and has a width greater than a width of the gate electrode.

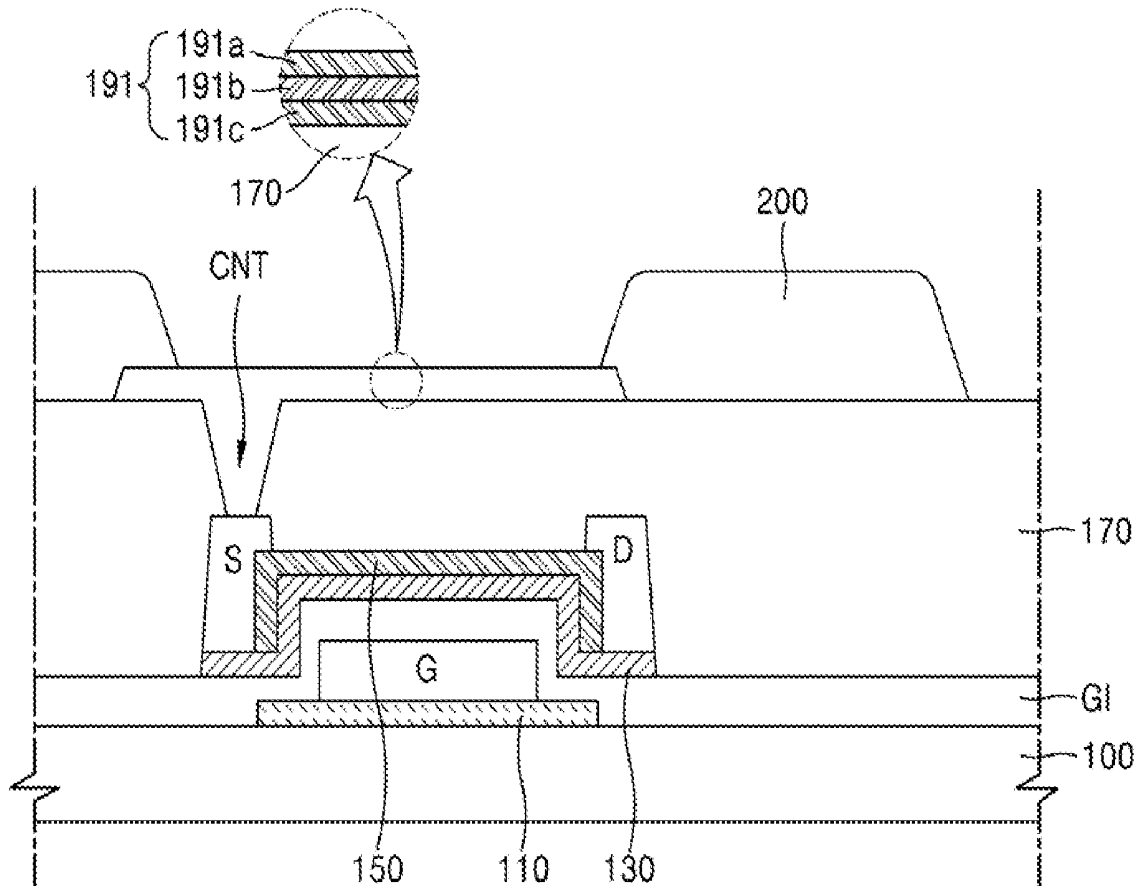


FIG. 1

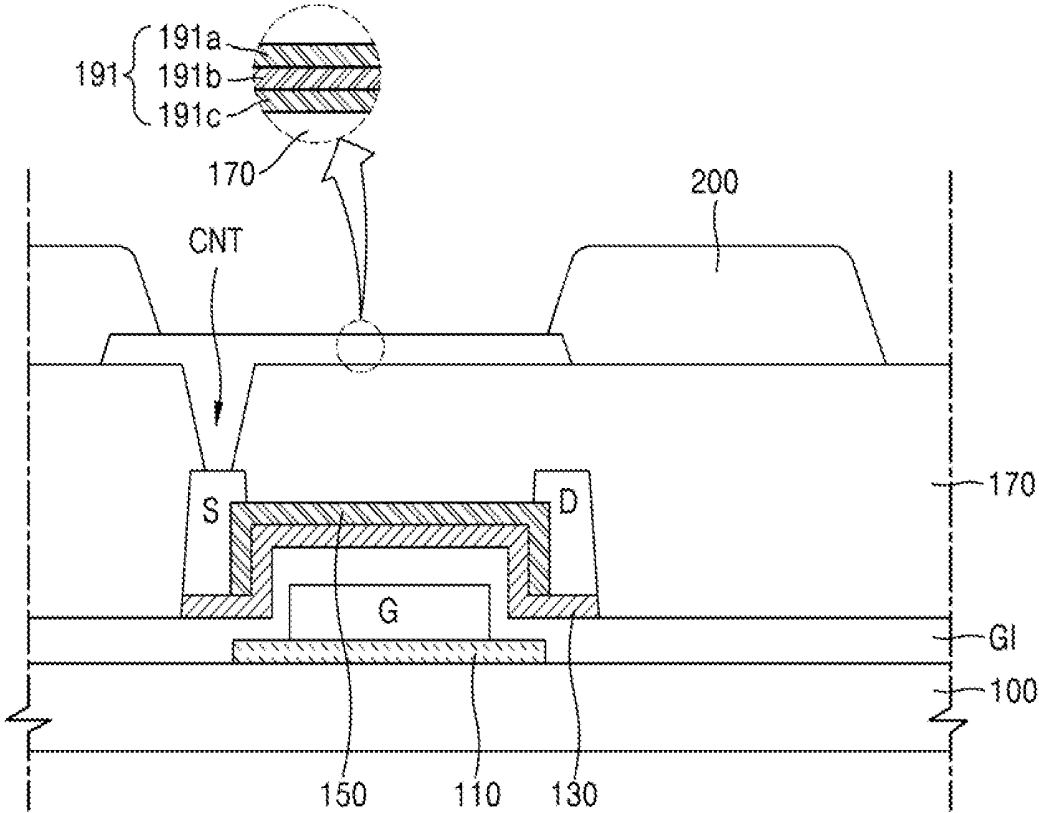


FIG. 2A

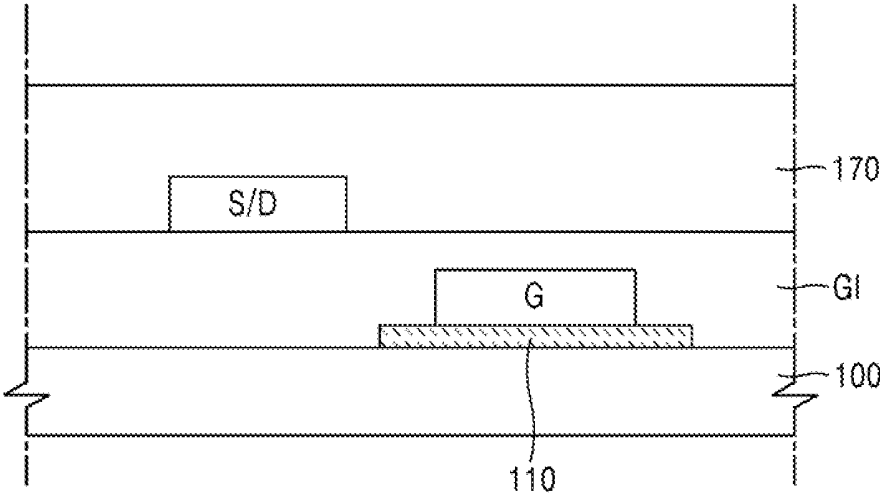


FIG. 2B

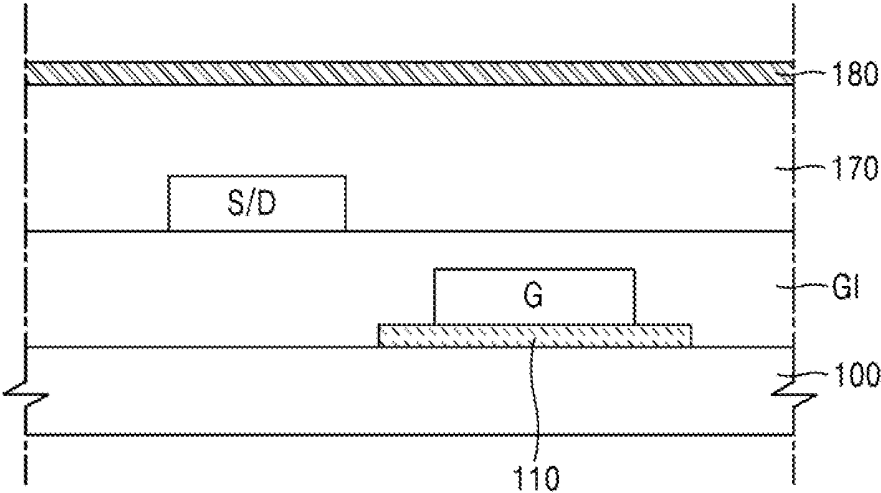


FIG. 2C

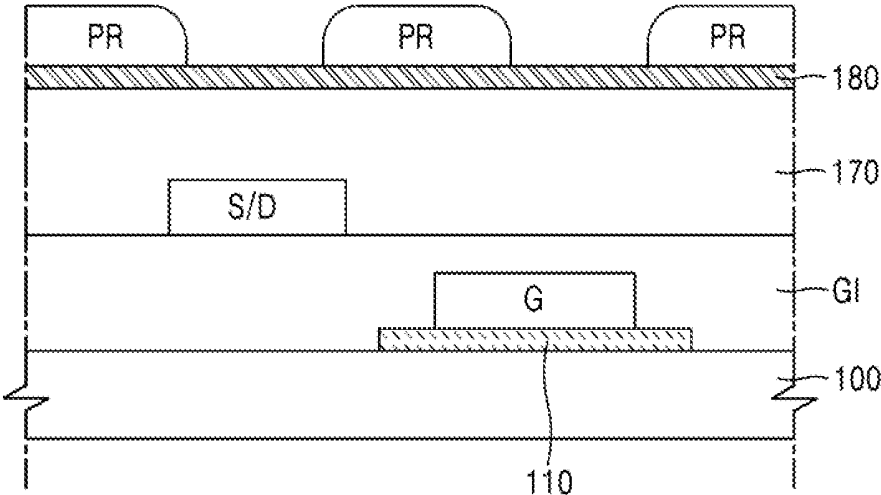




FIG. 3

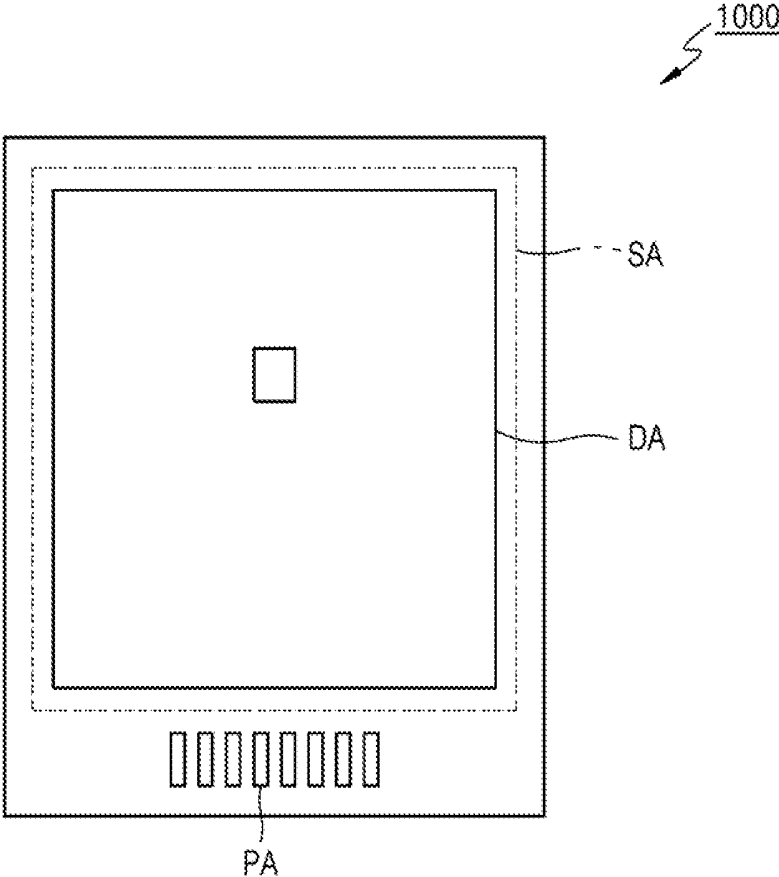
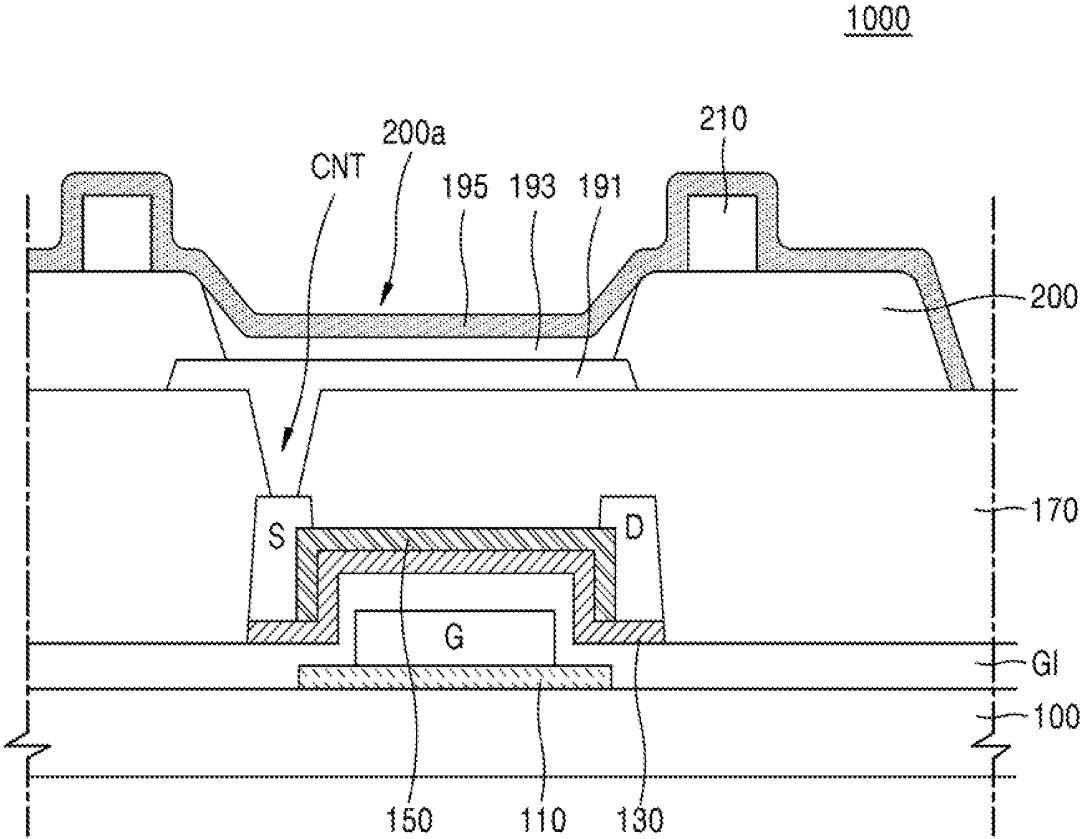


FIG. 4



**THIN-FILM TRANSISTOR ARRAY  
SUBSTRATE AND ORGANIC  
LIGHT-EMITTING DISPLAY INCLUDING  
THE SAME**

CROSS-REFERENCE TO RELATED  
APPLICATIONS

[0001] This application claims priority under 35 U.S.C. §119 to Korean Patent Application No. 10-2015-0055346, filed on Apr. 20, 2015, the disclosure of which is incorporated by reference herein in its entirety.

TECHNICAL FIELD

[0002] Exemplary embodiments of the inventive concept relate to a thin-film transistor (TFT) array substrate and an organic light-emitting display including the same.

DISCUSSION OF THE RELATED ART

[0003] An organic light-emitting display includes a hole injection electrode, an electron injection electrode, and an organic light-emitting device (OLED) including an organic emission layer that is formed between the hole injection electrode and the electron injection electrode. The organic light-emitting display is a self-emissive display that generates light when excitons generated when holes injected from the hole injection electrode and electrons injected from the electron injection electrode combine with each other in the organic emission layer and change from an excited state to a ground state.

[0004] The self-emissive organic light-emitting display does not require an additional light source, and thus, may operate with a low voltage and may have a light and thin design. Further, the organic light-emitting display has excellent characteristics such as a wide viewing angle, a high contrast ratio, and a fast response time.

SUMMARY

[0005] According to an exemplary embodiment of the inventive concept, a thin-film transistor (TFT) array substrate includes a substrate, a gate-underlying stepped layer disposed on the substrate, a gate electrode disposed on the gate-underlying stepped layer, a semiconductor layer formed over the gate electrode, and an etch-stopper disposed on the semiconductor layer. The gate-underlying stepped layer is formed under the gate electrode and has a width greater than a width of the gate electrode.

[0006] In an exemplary embodiment, the etch-stopper has a width about equal to or greater than the width of the gate-underlying stepped layer.

[0007] In an exemplary embodiment, ends of the etch-stopper are formed at positions corresponding to ends of the gate-underlying stepped layer, and the ends of the etch-stopper cover stepped portions of the gate electrode and the gate-underlying stepped layer.

[0008] In an exemplary embodiment, the TFT array substrate further includes a source electrode and a drain electrode disposed over the etch-stopper. The source electrode and the drain electrode are formed at positions corresponding to ends of the gate-underlying stepped layer.

[0009] In an exemplary embodiment, the TFT array substrate further includes a via layer formed over the source electrode and the drain electrode and covering an entire surface of the substrate.

[0010] In an exemplary embodiment, the via layer includes a contact hole at least partially exposing the source electrode and the drain electrode. The via layer and the contact hole are formed using one mask.

[0011] In an exemplary embodiment, the TFT array substrate further includes a source electrode and a drain electrode disposed over the etch-stopper. A distance between the source electrode and the drain electrode corresponds to the width of the gate-underlying stepped layer.

[0012] In an exemplary embodiment, the TFT array substrate further includes a via layer formed over the source electrode and the drain electrode and covering an entire surface of the substrate.

[0013] In an exemplary embodiment, the via layer further includes a contact hole at least partially exposing the source electrode and the drain electrode. The via layer and the contact hole are formed using one mask.

[0014] In an exemplary embodiment, the TFT array substrate further includes a gate insulating film disposed between the gate electrode and the semiconductor layer.

[0015] According to an exemplary embodiment of the inventive concept, a thin-film transistor (TFT) array substrate includes a substrate, a gate-underlying stepped layer disposed on the substrate, a gate electrode disposed on the gate-underlying stepped layer, an oxide semiconductor layer formed over the gate electrode, and an etch-stopper disposed on the oxide semiconductor layer. The etch-stopper has a width about equal to or greater than a width of the gate-underlying stepped layer.

[0016] In an exemplary embodiment, the gate-underlying stepped layer is disposed under the gate electrode, and the width of the gate-underlying stepped layer is about equal to or greater than a width of the gate electrode.

[0017] In an exemplary embodiment, the TFT array substrate further includes a via layer formed over the source electrode and the drain electrode and covering an entire surface of the substrate.

[0018] In an exemplary embodiment, the via layer includes a contact hole at least partially exposing the source electrode and the drain electrode, and the via layer and the contact hole are formed using one mask.

[0019] In an exemplary embodiment, the TFT array substrate further includes a source electrode and a drain electrode disposed over the etch-stopper. The source electrode and the drain electrode are formed at positions corresponding to ends of the gate-underlying stepped layer.

[0020] In an exemplary embodiment, the TFT array substrate further includes a via layer formed over the source electrode and the drain electrode and covering an entire surface of the substrate.

[0021] In an exemplary embodiment, the via layer includes a contact hole at least partially exposing the source electrode and the drain electrode, and the via layer and the contact hole are formed using one mask.

[0022] In an exemplary embodiment, the TFT array substrate further includes a source electrode and a drain electrode disposed over the etch-stopper. A distance between the source electrode and the drain electrode corresponds to the width of the gate-underlying stepped layer.

[0023] According to an exemplary embodiment of the inventive concept, a thin-film transistor (TFT) array substrate includes a substrate, a gate-underlying stepped layer disposed on the substrate, a gate electrode disposed on the gate-underlying stepped layer, an oxide semiconductor layer

formed over the gate electrode, and an etch-stopper disposed on the oxide semiconductor layer. Ends of the etch-stopper are formed at positions corresponding to ends of the gate-underlying stepped layer, and the ends of the etch-stopper cover stepped portions of the gate-underlying stepped layer and the gate electrode.

**[0024]** According to an exemplary embodiment of the inventive concept, an organic light-emitting display includes a display area including a plurality of pixels, and a non-display area disposed around the display area. Each of the plurality of pixels includes a substrate, a gate-underlying stepped layer disposed on the substrate, a gate electrode disposed on the gate-underlying stepped layer, an oxide semiconductor layer formed over the gate electrode, and an etch-stopper disposed on the oxide semiconductor layer. The gate-underlying stepped layer is formed under the gate electrode and has a width greater than a width of the gate electrode.

**[0025]** In an exemplary embodiment, the etch-stopper has a width about equal to or greater than the width of the gate-underlying stepped layer.

**[0026]** In an exemplary embodiment, ends of the etch-stopper are formed at positions corresponding to ends of the gate-underlying stepped layer, and the ends of the etch-stopper cover stepped portions of the gate electrode and the gate-underlying stepped layer.

**[0027]** In an exemplary embodiment, the organic light-emitting display further includes a source electrode and a drain electrode disposed over the etch-stopper. The source electrode and the drain electrode are formed at positions corresponding to ends of the gate-underlying stepped layer.

**[0028]** In an exemplary embodiment, the organic light-emitting display further includes a via layer formed over the source electrode and the drain electrode and covering an entire surface of the substrate.

**[0029]** In an exemplary embodiment, the via layer includes a contact hole at least partially exposing the source electrode and the drain electrode, and the via layer and the contact hole are formed using one mask.

**[0030]** In an exemplary embodiment, the organic light-emitting display further includes a source electrode and a drain electrode disposed over the etch-stopper. A distance between the source electrode and the drain electrode corresponds to the width of the gate-underlying stepped layer.

**[0031]** In an exemplary embodiment, the organic light-emitting display further includes a via layer formed over the source electrode and the drain electrode and covering an entire surface of the substrate.

**[0032]** In an exemplary embodiment, the via layer includes a contact hole at least partially exposing the source electrode and the drain electrode and the via layer and the contact hole are formed using one mask.

**[0033]** In an exemplary embodiment, the organic light-emitting display further includes a gate insulating film disposed between the gate electrode and the oxide semiconductor layer.

**[0034]** According to an exemplary embodiment of the inventive concept, an organic light-emitting display includes a display area including a plurality of pixels, and a non-display area disposed around the display area. Each of the plurality of pixels includes a substrate, a gate-underlying stepped layer disposed on the substrate, a gate electrode disposed on the gate-underlying stepped layer, an oxide semiconductor layer formed over the gate electrode, and an

etch-stopper disposed on the oxide semiconductor layer. The etch-stopper has a width about equal to or greater than a width of the gate-underlying stepped layer.

**[0035]** According to an exemplary embodiment of the inventive concept, a method of forming a thin-film transistor (TFT) array substrate includes forming a substrate, forming a gate-underlying stepped layer on the substrate, forming a gate electrode on the gate-underlying stepped layer, forming a semiconductor layer over the gate electrode, and forming an etch-stopper on the semiconductor layer. The gate-underlying stepped layer is formed under the gate electrode and has a width greater than a width of the gate electrode.

**[0036]** In an exemplary embodiment, the method further includes forming a source electrode and a drain electrode over the etch-stopper at positions corresponding to ends of the gate-underlying stepped layer, forming a via layer over the source electrode and the drain electrode, and forming a contact hole at least partially exposing the source electrode and the drain electrode. The via layer covers an entire surface of the substrate, and the via layer and the contact hole are formed using one mask.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0037]** The above and other features will become more apparent by describing in detail exemplary embodiments thereof with reference to the accompanying drawings, in which:

**[0038]** FIG. 1 is a cross-sectional view of a thin-film transistor (TFT) array substrate according to an exemplary embodiment of the inventive concept.

**[0039]** FIGS. 2A through 2D are cross-sectional views illustrating a process of forming a via layer and a contact hole in a TFT array substrate according to an exemplary embodiment of the inventive concept.

**[0040]** FIG. 3 is a plan view of an organic light-emitting display according to an exemplary embodiment of the inventive concept.

**[0041]** FIG. 4 is a cross-sectional view of the organic light-emitting display of FIG. 3 according to an exemplary embodiment of the inventive concept.

#### DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

**[0042]** Exemplary embodiments of the present inventive concept will be described more fully hereinafter with reference to the accompanying drawings. In the drawings, the size and relative sizes of layers and regions may be exaggerated for clarity. Like reference numerals may refer to like elements throughout the accompanying drawings.

**[0043]** It will be understood that although the terms “first”, “second”, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These elements are only used to distinguish one element from another. Thus, a “first” element in an exemplary embodiment may be described as a “second” element in another exemplary embodiment.

**[0044]** It will be understood that when a component, such as a film, a region, a layer, or an element, is referred to as being “on”, “connected to”, “coupled to”, or “adjacent to” another component, it can be directly on, connected, coupled, or adjacent to the other component, or intervening components may be present. It will also be understood that when a component is referred to as being “between” two

components, it can be the only component between the two components, or one or more intervening components may also be present. It will also be understood that when a component is referred to as “covering” another component, it can be the only component covering the other component, or one or more intervening components may also be covering the other component.

[0045] When a certain embodiment may be implemented differently, a specific process order may be performed differently from the described order. For example, two consecutively described processes may be performed substantially at the same time or performed in an order opposite to the described order.

[0046] As used herein, the term “and/or” includes any and all combinations of one or more of the associated listed items.

[0047] Herein, when two or more elements or values are described as being substantially the same as or equal to each other, it is to be understood that the elements or values are identical to each other, indistinguishable from each other, or distinguishable from each other but functionally the same as each other as would be understood by a person having ordinary skill in the art. Further, when processes are described as being performed at substantially the same time, it is to be understood that the processes may be performed at exactly the same time or at about the same time as would be understood by a person having ordinary skill in the art.

[0048] Spatially relative terms, such as “beneath”, “below”, “lower”, “under”, “above”, “upper” and the like, may be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. It will be understood that the spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as “below” or “beneath” or “under” other elements or features would then be oriented “above” the other elements or features. Thus, the exemplary terms “below” and “under” can encompass both an orientation of above and below. In addition, it will also be understood that when a layer is referred to as being “between” two layers, it can be the only layer between the two layers, or one or more intervening layers may also be present.

[0049] FIG. 1 is a cross-sectional view of a thin-film transistor (TFT) array substrate according to an exemplary embodiment of the inventive concept.

[0050] Referring to FIG. 1, the TFT array substrate according to an exemplary embodiment may include a substrate 100, a gate-underlying stepped layer 110, a gate electrode G, a semiconductor layer 130, and an etch-stopper 150 provided on the substrate 100.

[0051] The substrate 100 may be formed of a transparent material such as, for example, glass. However, the substrate 100 is not limited thereto.

[0052] The gate-underlying stepped layer 110 may be provided over the substrate 100 to be located under the gate electrode G. For example, the gate-underlying stepped layer 110 may be disposed between the substrate 100 and the gate electrode G. As shown in FIG. 1, according to an exemplary embodiment, the gate-underlying stepped layer 110 may be formed to have a width greater than a width of the gate electrode G.

[0053] The gate-underlying stepped layer 110 may prevent poor step coverage. For example, without the gate-underlying stepped layer 110, poor step coverage may occur. That is, when only the gate electrode G is formed over the substrate 100 without the gate-underlying stepped layer 110, poor step coverage may occur.

[0054] For example, when only the gate electrode G is formed, a large stepped portion may be formed between the substrate 100 and both ends of the gate electrode G. For example, the sides of the gate electrode G extending from the upper surface of the gate electrode G downward toward the substrate 100 may be large when only the gate electrode G is formed. This large stepped portion may increase as a stack increases, thereby resulting in poor step coverage.

[0055] In the TFT array substrate according to exemplary embodiments of the inventive concept, since the gate-underlying stepped layer 110 (e.g., one stepped portion) is formed under the gate electrode G, and since the gate-underlying stepped layer 110 (e.g., the one stepped portion) is further formed between the substrate 100 and both ends of the gate electrode G, the stepped portions as a whole and poor step coverage may be reduced.

[0056] The material of the gate electrode G may include at least one metal selected from among, for example, molybdenum (Mo), aluminum (Al), platinum (Pt), palladium (Pd), silver (Ag), magnesium (Mg), gold (Au), nickel (Ni), neodymium (Nd), iridium (Ir), chromium (Cr), lithium (Li), calcium (Ca), titanium (Ti), tungsten (W), and copper (Cu). However, the material of the gate electrode G is not limited thereto.

[0057] A gate insulating film GI may be formed over the gate electrode G, and may be formed to correspond to an entire surface of the substrate 100. That is, the gate insulating film GI may cover an entirety of the substrate 100. The gate insulating film GI may be formed to have a multi-layer or single-layer structure formed of an inorganic material such as, for example, silicon oxide or silicon nitride. However, the gate insulating film GI is not limited thereto. The gate insulating film GI may insulate the gate electrode G from the semiconductor layer 130, which may be provided over the gate insulating film GI.

[0058] In an exemplary embodiment, the semiconductor layer 130 includes a transparent conductive oxide. The transparent conductive oxide may include, for example, at least one element selected from among gallium (Ga), indium (In), zinc (Zn), hafnium (Hf), and tin (Sn). For example, the transparent conductive oxide may be selected from InGaZnO, ZnSnO, InZnO, InGaO, ZnO, TiO, and hafnium-indium-zinc oxide (HIZO). However, exemplary embodiments of the inventive concept are not limited thereto. Since a TFT including a silicon oxide layer is typically formed using a high-temperature process and undergoes a crystallization process, as the size of the TFT increases, uniformity may be reduced during the crystallization process, thereby making it difficult to increase the size of the TFT.

[0059] However, since an oxide semiconductor TFT including a transparent conductive oxide has excellent device characteristics and may be formed using a low-temperature process, the oxide semiconductor TFT may be used for a backplane for a flat panel display. Further, since the oxide semiconductor TFT is transparent in a visible region and is flexible, the oxide semiconductor TFT may be applied to a transparent display or a flexible display.

[0060] The etch-stopper 150 may be formed over the semiconductor layer 130 as shown in FIG. 1. The etch-stopper 150 may be formed between the gate electrode G and a source electrode S and/or a drain electrode D disposed over the etch-stopper 150, and may protect the semiconductor layer 130.

[0061] For example, when the semiconductor layer 130 is formed of an oxide as described above, to ensure high stability, the TFT array substrate may include the etch-stopper 150 to protect a top surface from an etching solution. The etch-stopper 150 may be formed to protect the semiconductor layer 130 from the etching solution that is introduced through a gap between the source electrode S and the drain electrode D.

[0062] In the TFT array substrate according to an exemplary embodiment, the etch-stopper 150 may be formed to have a width corresponding to the width of the gate-underlying stepped layer 110. That is, the etch-stopper 150 may be formed so that both ends of the etch-stopper 150 extend to positions corresponding to both ends of the gate-underlying stepped layer 110. For example, the ends of the etch-stopper 150 may align with the ends of the gate-underlying stepped layer 110.

[0063] Since the etch-stopper 150 is formed to extend to a stepped portion of the gate electrode G, a structure in which two insulating layers are formed may be formed between the gate electrode G and the source and drain electrodes S and D.

[0064] That is, since the gate insulating film GI and the etch-stopper 150 are disposed as two insulating layers between the gate electrode G and the source and drain electrodes S and D, parasitic capacitance between the gate electrode G and the source and drain electrodes S and D may be reduced. As a result, a wiring load in a gate wiring and a data wiring may be reduced, thereby leading to high image quality.

[0065] The etch-stopper 150 may be formed to cover all stepped portions formed by the gate electrode G and the gate-underlying stepped layer 110, as described above.

[0066] In a comparative example, an etch-stopper is formed to have a width corresponding to the width of the gate electrode G. In this case, in order not to expose the semiconductor layer 130, a distance between the source electrode S and the drain electrode D is reduced.

[0067] In this case, the source electrode S and the drain electrode D are formed close to each other. As a result, an overlapped portion may be formed between the source and drain electrodes S and D and the gate electrode G, and parasitic capacitance of a transistor may occur in the overlapped portion, thereby resulting in coupling.

[0068] However, in the TFT array substrate according to exemplary embodiments of the inventive concept, since the etch-stopper 150 is formed to have a width corresponding to the width of the gate-underlying stepped layer 110, the source electrode S and the drain electrode D may be formed to have a predetermined distance therebetween without damaging the semiconductor layer 130.

[0069] That is, since the etch-stopper 150 may cover all stepped portions of the gate electrode G and the gate-underlying stepped layer 110 in exemplary embodiments, parasitic capacitance may be reduced.

[0070] Since the etch-stopper 150 is formed to cover all stepped portions of the gate-underlying stepped layer 110 as

described above, the source electrode S and the drain electrode D may be formed to have a predetermined distance therebetween.

[0071] For example, a distance between the source electrode S and the drain electrode D may be maintained to correspond to the width of the gate-underlying stepped layer 110. That is, the source electrode S and the drain electrode D may be formed at positions corresponding to the both ends of the gate-underlying stepped layer 110 (e.g., the source electrode S and the drain electrode D may substantially align with the ends of the gate-underlying stepped layer 110). For example, the distance between the source electrode S and the drain electrode D may be about equal to the width of the gate-underlying stepped layer 110.

[0072] In a comparative example of a TFT array substrate, since the gate-underlying stepped layer 110 is not formed, when the source electrode S and the drain electrode D are formed to have a predetermined distance therebetween, an offset area is formed.

[0073] However, in the TFT array substrate according to exemplary embodiments of the inventive concept, since the gate-underlying stepped layer 110 is formed under the gate electrode G, and the source electrode S and the drain electrode D are formed to have a distance corresponding to the width of the gate-underlying stepped layer 110, the source electrode S and the drain electrode D may be formed to have a large distance therebetween without forming an offset area, thereby reducing parasitic capacitance.

[0074] A via layer 170 may be formed over the etch-stopper 150 and the source and drain electrodes S and D to correspond to the entire surface of the substrate 100. That is, the via layer 170 may cover an entirety of the substrate 100.

[0075] The via layer 170 may be formed of an inorganic material or an organic material. The via layer 170 may be formed, for example, of at least one material selected from an acryl-based resin, an epoxy resin, a phenolic resin, a polyamide-based resin, a polyimide-based resin, an unsaturated polyester-based resin, a polyphenylene-based resin, a polyphenylenesulfide-based resin, and benzoocyclobutene (BCB). However, exemplary embodiments of the inventive concept are not limited thereto.

[0076] A contact hole CNT may be formed in the via hole 170 as shown in FIG. 1.

[0077] The source electrode S and/or the drain electrode D may be exposed through the contact hole CNT. One of the source electrode S and the drain electrode D may be connected to a pixel electrode 191 through the contact hole CNT.

[0078] In the TFT array substrate according to an exemplary embodiment, the via layer 170 and the contact hole CNT may be formed using one mask instead of multiple masks.

[0079] Accordingly, the TFT array substrate may be formed by using fewer masks than those used to form a TFT array substrate in comparative examples, as described further below.

[0080] The pixel electrode 191, which is connected to any one of the source electrode S and the drain electrode D through the contact hole CNT, may be formed over the via layer 170.

[0081] The pixel electrode 191 may include a semi-transparent metal layer 191b, a first transparent conductive oxide layer 191a that is formed over the semi-transparent metal

layer **191b**, and a second transparent conductive oxide layer **191c** that is formed under the semi-transparent metal layer **191b**.

[0082] The semi-transparent metal layer **191b** may be formed of, for example, silver (Ag) or an Ag alloy. Since the semi-transparent metal layer **191b** forms a micro-cavity structure along with a counter electrode **195** (see FIG. 4) that may be a reflective electrode, the luminous efficiency of an organic light-emitting display including the TFT array substrate according to exemplary embodiments of the inventive concept may be improved.

[0083] Each of the first and second transparent conductive oxide layers **191a** and **191c** may include, for example, at least one selected from among indium tin oxide (ITO), indium zinc oxide (IZO), zinc oxide (ZnO), indium oxide ( $\text{In}_2\text{O}_3$ ), indium gallium oxide (IGO), and aluminum zinc oxide (AZO). However, exemplary embodiments of the inventive concept are not limited thereto. The first transparent conductive oxide layer **191a** may increase an adhesive force between the via layer **170** and the semi-transparent metal layer **191b**, and the second transparent conductive oxide layer **191c** may function as a barrier layer that protects the semi-transparent metal layer **191b**.

[0084] FIGS. 2A through 2D are cross-sectional views illustrating a process of forming the via layer **170** and the contact hole CNT in the TFT array substrate according to an exemplary embodiment of the inventive concept.

[0085] According to an exemplary embodiment, the via layer **170** and the contact hole CNT may be formed using one mask through metal masking. However, the method of forming the via layer **170** and the contact hole CNT is not limited thereto. For example, the via layer **170** and the contact hole CNT may be formed using one mask through a multi-PR process.

[0086] As shown in FIGS. 2A through 2D, in the TFT array substrate according to an exemplary embodiment, the via layer **170** and the contact hole CNT may be formed using one mask through metal masking.

[0087] Referring to FIG. 2A, first, the via layer **170** may be formed over the entire surface of the substrate **100** to cover the source electrode and/or the drain electrode S/D.

[0088] Next, referring to FIG. 2B, a metal layer **180** may be additionally deposited over the via layer **170** allowing for the etching of the via layer **170** and the gate insulating film GI at one time in a subsequent etching process.

[0089] Next, referring to FIG. 2C, exposure is performed using one mask (e.g., photoresist mask PR). As shown in FIG. 2D, the via layer **170** and the gate insulating film GI may be etched to form the contact hole CNT at one time. That is, the via layer **170** and the gate insulating film GI may be etched to form the contact hole CNT as substantially the same time.

[0090] Further, the metal layer **180** may be removed in a subsequent process.

[0091] Thus, according to exemplary embodiments of the inventive concept, the via layer **170** and the contact hole CNT in a TFT array substrate may be formed using one mask, resulting in a reduction in fabrication time and cost.

[0092] According to exemplary embodiments of the inventive concept, a method of forming a TFT array substrate includes forming the substrate **100**, forming the gate-underlying stepped layer **110** on the substrate **100**, forming the gate electrode G on the gate-underlying stepped layer **110**, forming the semiconductor layer **130** over the gate

electrode G, and forming the etch-stopper **150** on the semiconductor layer **130**. As described above, the gate-underlying stepped layer **110** is formed under the gate electrode G and has a width greater than a width of the gate electrode G. The method may further include forming the source electrode S and the drain electrode D over the etch-stopper **150** at positions corresponding to ends of the gate-underlying stepped layer **110**, forming the via layer **170** over the source electrode S and the drain electrode D, and forming the contact hole CNT at least partially exposing the source electrode S and the drain electrode D. As described above, the via layer **170** and the contact hole CNT may be formed using one mask, and the via layer **170** covers an entire surface of the substrate **100**.

[0093] FIG. 3 is a plan view of an organic light-emitting display **1000** according to an exemplary embodiment of the inventive concept. FIG. 4 is a cross-sectional view of the organic light-emitting display **1000** of FIG. 3 according to an exemplary embodiment of the inventive concept. In FIGS. 3 and 4, elements previously described with reference to FIGS. 1 through 2D are denoted by the same reference numerals, and for convenience of description, a repeated explanation thereof may be omitted herein.

[0094] As shown in FIG. 3, the organic light-emitting display **1000** may be divided into a display area DA in which an image is displayed, and a non-display area around the display area DA in which an image is not displayed. The non-display area includes a sealing area SA and a pad area PA.

[0095] A sealing substrate and/or a sealing material may be disposed in the sealing area SA and may surround the display area DA. However, exemplary embodiments of the inventive concept are not limited thereto. For example, any configuration in which the sealing substrate and/or the sealing material seal the display area DA may be utilized according to exemplary embodiments.

[0096] The sealing substrate may be, for example, a thin-film encapsulation substrate. In this case, the sealing material may be omitted. The sealing substrate may prevent external moisture or air from penetrating into a plurality of TFTs and an OLED that are disposed on the substrate **100**. A polarization film or a color filter may be further provided on the sealing substrate as desired.

[0097] The sealing material may be an inorganic material such as, for example, a frit. However, exemplary embodiments of the inventive concept are not limited thereto. For example, the sealing material may be epoxy. The sealing material may be coated using a dispenser or screen printing. The frit may refer to a raw material in a powder state used to form a glass, or may encompass a material in a paste state obtained by adding a laser or infrared absorber, an organic binder, or a filler for reducing a thermal expansion coefficient to a main material such as  $\text{SiO}_2$ . The frit in the paste state may be cured as the organic binder and moisture are removed during drying or firing. The laser or infrared absorber may include a transition metal compound. A laser beam may be used as a heat source for curing the sealing material and attaching the substrate **100** to the sealing substrate. A light-absorbing layer that assists in absorbing the laser beam during the curing using the laser beam may be further disposed under the sealing material. The light-absorbing layer may be formed of a conductive material having a high heat transfer coefficient.

[0098] The pad area PA refers to an area in which various members that drive pixels provided in the display area DA and other modules are mounted.

[0099] The OLED is provided on the substrate 100 in the display area DA. The OLED includes the pixel electrode 191, an intermediate layer 193 that includes an organic emission layer, and the counter electrode 195. The organic light-emitting display 1000 may further include a pixel-defining film 200 and spacers 210.

[0100] The pixel electrode 191 may be electrically connected to the source electrode S or the drain electrode D by filling the contact hole CNT of the via layer 170.

[0101] However, exemplary embodiments of the present inventive concept are not limited thereto. For example, in exemplary embodiments, a contact metal may be provided, the source electrode S or the drain electrode D may contact the contact metal, and the pixel electrode 191 may be electrically connected to the contact metal.

[0102] The pixel electrode 191 and/or the counter electrode 195 may be, for example, a transparent electrode or a reflective electrode. When the pixel electrode 191 and/or the counter electrode 195 is a transparent electrode, the pixel electrode 191 and/or the counter electrode may be formed of, for example, ITO, IZO, ZnO, or  $\text{In}_2\text{O}_3$ . When the pixel electrode 191 and/or the counter electrode 195 is a reflective electrode, the pixel electrode 191 and/or the counter electrode 195 may include, for example, a reflective film formed of Ag, Mg, Al, Pt, Pd, Au, Ni, Nd, Ir, Cr, or a compound thereof, and a transparent film formed of ITO, IZO, ZnO, or  $\text{In}_2\text{O}_3$ . In exemplary embodiments, the pixel electrode 191 and/or the counter electrode 195 may have an ITO/Ag/ITO structure.

[0103] The pixel-defining film 200 may define a pixel region and a non-pixel region. The pixel-defining film 200 may include an opening 200a through which the pixel electrode 191 is exposed, and may be formed to entirely cover the substrate 100. The intermediate layer 193 may be formed in the opening 200a, and the opening 200a may substantially occupy the pixel region.

[0104] The pixel electrode 191, the intermediate layer 193, and the counter electrode 195 constitute the OLED. Holes and electrons injected from the pixel electrode 191 and the counter electrode 195 of the OLED combine with each other in the organic emission layer of the intermediate layer 193 to generate light.

[0105] In an exemplary embodiment, the intermediate layer 193 may include only the organic emission layer. Alternatively, the intermediate layer 193 may include the organic emission layer and may further include at least one of a hole injection layer (HIL), a hole transport layer (HTL), an electron transport layer (ETL), and an electron injection layer (EIL). However, exemplary embodiments of the inventive concept are not limited thereto. For example, the intermediate layer 193 may include the organic emission layer and may further include other various functional layers.

[0106] The counter electrode 195 is formed on the intermediate layer 193. The counter electrode 195 may form an electric field with the pixel electrode 191 and may assist in the emission of light from the intermediate layer 193. The pixel electrode 191 may be patterned for each pixel, and the counter electrode 195 may be formed so that a common voltage is applied to all pixels. The counter electrode 195 may also be referred to as a common electrode 195.

[0107] Each of the pixel electrode 191 and the counter electrode 195 may be, for example, a transparent electrode or a reflective electrode. The pixel electrode 191 may function as an anode and the counter electrode 195 may function as a cathode. However, exemplary embodiments of the present inventive concept are not limited thereto. For example, the pixel electrode 191 may function as a cathode and the counter electrode 195 may function as an anode.

[0108] Although only one OLED is illustrated in FIG. 4, a display panel may include a plurality of the OLEDs. For example, one pixel may be formed for each of the OLEDs, and each pixel may emit red, green, blue, or white light.

[0109] However, exemplary embodiments of the present inventive concept are not limited thereto. For example, the intermediate layer 193 may be commonly formed over the pixel electrode 191 irrespective of a position of a pixel. In this case, the organic emission layer may be formed by vertically stacking or combining layers including light-emitting materials that emit, for example, red, green, and blue light. Other combinations that are capable of emitting white light may also be utilized. Further, according to exemplary embodiments, a color conversion layer or a color filter that converts the emitted white light into predetermined color light may be further provided.

[0110] A protective layer may be disposed on the counter electrode 195, and may cover and protect the OLED. The protective layer may be, for example, an inorganic insulating film and/or an organic insulating film.

[0111] The spacers 210 may be disposed between pixel regions in the display area DA. The spacers 210 may maintain a distance between the substrate 100 and the sealing substrate, and may prevent display characteristics from being deteriorated due to external impact.

[0112] The spacers 210 may be provided on the pixel-defining film 200. The spacers 210 may protrude from the pixel-defining film 200 toward the sealing substrate.

[0113] In exemplary embodiments, the spacers 210 may be formed of the same material by using the same process as those of the pixel-defining film 200. That is, the pixel-defining film 200 and the spacers 210 may be simultaneously formed at substantially the same time by adjusting the amount of light through an exposure process using a half-tone mask. However, exemplary embodiments of the present inventive concept are not limited thereto. For example, in exemplary embodiments, the pixel-defining film 200 and the spacers 210 may be sequentially or individually formed, and thus, may be independent structures formed using different materials.

[0114] As described above, in the organic light-emitting display 1000 according to an exemplary embodiment of the present inventive concept, since the gate-underlying stepped layer 110 is formed under the gate electrode G and a stepped portion of the gate electrode G is reduced, poor step coverage may be prevented/reduced. In addition, since the etch-stopper 150 extends to cover both ends of the gate-underlying stepped layer 110, a wiring load may be reduced and parasitic capacitance may be reduced/minimized. In addition, since the via layer 170 and the contact hole CNT are formed using one mask, the number of mask processes may be reduced, resulting in a reduction of the time and cost involved in manufacturing an organic light-emitting display.

[0115] According to exemplary embodiments of the inventive concept, since a gate-underlying stepped layer is formed, poor step coverage that occurs due to a stepped portion may be prevented.

[0116] Further, since an etch-stopper extends to have a width corresponding to a width of the gate-underlying stepped layer, a wiring load may be reduced.

[0117] While the present inventive concept has been particularly shown and described with reference to the exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the present inventive concept as defined by the following claims.

What is claimed is:

1. A thin-film transistor (TFT) array substrate, comprising:

a substrate;  
a gate-underlying stepped layer disposed on the substrate;  
a gate electrode disposed on the gate-underlying stepped layer;  
a semiconductor layer formed over the gate electrode; and  
an etch-stopper disposed on the semiconductor layer,  
wherein the gate-underlying stepped layer is formed under the gate electrode and has a width greater than a width of the gate electrode.

2. The TFT array substrate of claim 1, wherein the etch-stopper has a width about equal to or greater than the width of the gate-underlying stepped layer.

3. The TFT array substrate of claim 1, wherein ends of the etch-stopper are formed at positions corresponding to ends of the gate-underlying stepped layer, and the ends of the etch-stopper cover stepped portions of the gate electrode and the gate-underlying stepped layer.

4. The TFT array substrate of claim 1, further comprising:  
a source electrode and a drain electrode disposed over the etch-stopper,  
wherein the source electrode and the drain electrode are formed at positions corresponding to ends of the gate-underlying stepped layer.

5. The TFT array substrate of claim 4, further comprising:  
a via layer formed over the source electrode and the drain electrode and covering an entire surface of the substrate.

6. The TFT array substrate of claim 5, wherein the via layer comprises:

a contact hole at least partially exposing the source electrode and the drain electrode,  
wherein the via layer and the contact hole are formed using one mask.

7. The TFT array substrate of claim 1, further comprising:  
a source electrode and a drain electrode disposed over the etch-stopper, wherein a distance between the source electrode and the drain electrode corresponds to the width of the gate-underlying stepped layer.

8. The TFT array substrate of claim 7, further comprising:  
a via layer formed over the source electrode and the drain electrode and covering an entire surface of the substrate.

9. The TFT array substrate of claim 8, wherein the via layer comprises:

a contact hole at least partially exposing the source electrode and the drain electrode,

wherein the via layer and the contact hole are formed using one mask.

10. The TFT array substrate of claim 1, further comprising:

a gate insulating film disposed between the gate electrode and the semiconductor layer.

11. A thin-film transistor (TFT) array substrate, comprising:

a substrate;  
a gate-underlying stepped layer disposed on the substrate;  
a gate electrode disposed on the gate-underlying stepped layer;  
an oxide semiconductor layer formed over the gate electrode; and  
an etch-stopper disposed on the oxide semiconductor layer,  
wherein the etch-stopper has a width about equal to or greater than a width of the gate-underlying stepped layer.

12. The TFT array substrate of claim 11, wherein the gate-underlying stepped layer is disposed under the gate electrode, and the width of the gate-underlying stepped layer is about equal to or greater than a width of the gate electrode.

13. The TFT array substrate of claim 12, further comprising:

a via layer formed over the source electrode and the drain electrode and covering an entire surface of the substrate.

14. The TFT array substrate of claim 13, wherein the via layer comprises a contact hole at least partially exposing the source electrode and the drain electrode, and the via layer and the contact hole are formed using one mask.

15. The TFT array substrate of claim 11, further comprising:

a source electrode and a drain electrode disposed over the etch-stopper,  
wherein the source electrode and the drain electrode are formed at positions corresponding to ends of the gate-underlying stepped layer.

16. The TFT array substrate of claim 15, further comprising:

a via layer formed over the source electrode and the drain electrode and covering an entire surface of the substrate.

17. The TFT array substrate of claim 16, wherein the via layer comprises a contact hole at least partially exposing the source electrode and the drain electrode, and the via layer and the contact hole are formed using one mask.

18. The TFT array substrate of claim 11, further comprising:

a source electrode and a drain electrode disposed over the etch-stopper,  
wherein a distance between the source electrode and the drain electrode corresponds to the width of the gate-underlying stepped layer.

19. A thin-film transistor (TFT) array substrate, comprising:

a substrate;  
a gate-underlying stepped layer disposed on the substrate;  
a gate electrode disposed on the gate-underlying stepped layer;  
an oxide semiconductor layer formed over the gate electrode; and

an etch-stopper disposed on the oxide semiconductor layer,

wherein ends of the etch-stopper are formed at positions corresponding to ends of the gate-underlying stepped layer, and the ends of the etch-stopper cover stepped portions of the gate-underlying stepped layer and the gate electrode.

**20.** An organic light-emitting display, comprising:

a display area comprising a plurality of pixels; and a non-display area disposed around the display area, wherein each of the plurality of pixels comprises: a substrate;

a gate-underlying stepped layer disposed on the substrate; a gate electrode disposed on the gate-underlying stepped layer;

an oxide semiconductor layer formed over the gate electrode; and

an etch-stopper disposed on the oxide semiconductor layer,

wherein the gate-underlying stepped layer is formed under the gate electrode and has a width greater than a width of the gate electrode.

**21.** The organic light-emitting display of claim **20**, wherein the etch-stopper has a width about equal to or greater than the width of the gate-underlying stepped layer.

**22.** The organic light-emitting display of claim **20**, wherein ends of the etch-stopper are formed at positions corresponding to ends of the gate-underlying stepped layer, and the ends of the etch-stopper cover stepped portions of the gate electrode and the gate-underlying stepped layer.

**23.** The organic light-emitting display of claim **20**, further comprising:

a source electrode and a drain electrode disposed over the etch-stopper,

wherein the source electrode and the drain electrode are formed at positions corresponding to ends of the gate-underlying stepped layer.

**24.** The organic light-emitting display of claim **23**, further comprising:

a via layer formed over the source electrode and the drain electrode and covering an entire surface of the substrate.

**25.** The organic light-emitting display of claim **24**, wherein the via layer comprises a contact hole at least partially exposing the source electrode and the drain electrode and the via layer and the contact hole are formed using one mask.

**26.** The organic light-emitting display of claim **20**, further comprising:

a source electrode and a drain electrode disposed over the etch-stopper,

wherein a distance between the source electrode and the drain electrode corresponds to the width of the gate-underlying stepped layer.

**27.** The organic light-emitting display of claim **26**, further comprising:

a via layer formed over the source electrode and the drain electrode and covering an entire surface of the substrate.

**28.** The organic light-emitting display of claim **27**, wherein the via layer comprises a contact hole at least partially exposing the source electrode and the drain electrode and the via layer and the contact hole are formed using one mask.

**29.** The organic light-emitting display of claim **20**, further comprising:

a gate insulating film disposed between the gate electrode and the oxide semiconductor layer.

**30.** An organic light-emitting display, comprising:

a display area comprising a plurality of pixels; and a non-display area disposed around the display area, wherein each of the plurality of pixels comprises:

a substrate;

a gate-underlying stepped layer disposed on the substrate;

a gate electrode disposed on the gate-underlying stepped layer;

an oxide semiconductor layer formed over the gate electrode; and

an etch-stopper disposed on the oxide semiconductor layer,

wherein the etch-stopper has a width about equal to or greater than a width of the gate-underlying stepped layer.

**31.** A method of forming a thin-film transistor (TFT) array substrate, comprising:

forming a substrate;

forming a gate-underlying stepped layer on the substrate;

forming a gate electrode on the gate-underlying stepped layer;

forming a semiconductor layer over the gate electrode; and

forming an etch-stopper on the semiconductor layer,

wherein the gate-underlying stepped layer is formed under the gate electrode and has a width greater than a width of the gate electrode.

**32.** The method of claim **31**, further comprising:

forming a source electrode and a drain electrode over the etch-stopper at positions corresponding to ends of the gate-underlying stepped layer;

forming a via layer over the source electrode and the drain electrode, wherein the via layer covers an entire surface of the substrate; and

forming a contact hole at least partially exposing the source electrode and the drain electrode, wherein the via layer and the contact hole are formed using one mask.

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